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ADVANCED PROBE CARD AND METHOD OF FABRICATING SAME

Inventors: Bo Jin and James E. Nulty

CROSS-REFERENCE TO RELATED APPLICATION

This application claims the benefit of U.S. Provisional Application No. 60/457,885, entitled "Method and Apparatus for Advanced Probe Card," filed on March 26, 2003 by Bo Jin and James E. Nulty, which is incorporated herein by reference in its entirety.

BACKGROUND OF THE INVENTION

1. Field Of The Invention

The present invention relates generally to integrated circuits, and more particularly but not exclusively to methods and apparatus for testing integrated circuits.

2. Description Of The Background Art

Probe cards are used in the testing of integrated circuits by providing an interface between the pads of a bare die or chip and the test equipment. Most probe cards are configured with probe pins that have tips including hard materials so that they can be repeatedly used to test different chips. Typical probe cards are commonly configured to be connected to only one chip at a time. So, where a wafer may contain hundreds of individual chips, only one chip location at a time could be tested using this approach.

Another disadvantage of this conventional approach is that the wafer itself typically receives some damage from the probe tip touch down. If there is substantial misalignment, some chips can be destroyed in this way.

SUMMARY

In one embodiment, an anti-wafer structure includes a silicon on insulator (SOI) layer and a plurality of probe dice formed on the SOI layer. Each of the probe die may have a pad layout corresponding to a pad layout of a die on a wafer under test. A plurality of holes may extend through the SOI layer and the plurality of probe dice, with each hole corresponding to a pad on a probe die. The anti-wafer structure may be advantageously used in an advanced probe card. Techniques for fabricating an anti-wafer and an advanced probe card are also disclosed.

These and other features of the present invention will be readily apparent to persons of ordinary skill in the art upon reading the entirety of this disclosure, which includes the accompanying drawings and claims.

DESCRIPTION OF THE DRAWINGS

FIG. 1 schematically shows an anti-wafer in accordance with an embodiment of the present invention.

FIG. 2 schematically shows a probe die in accordance with an embodiment of the present invention.

FIG. 3 schematically shows a cross-sectional view of an advanced probe card in accordance with an embodiment of the present invention.

FIG. 4 shows a cross-sectional view of an anti-wafer in accordance with an embodiment of the present invention.

FIG. 5 shows a portion of an advanced probe card in accordance with an embodiment of the present invention.

FIGS. 6-11 systematically illustrate the fabrication of an anti-wafer in accordance with an embodiment of the present invention

The use of the same reference label in different drawings indicates the same or like components. Drawings are not necessarily to scale unless otherwise noted.

DETAILED DESCRIPTION

In the present disclosure, numerous specific details are provided, such as examples of apparatus, components, and methods, to provide a thorough understanding of embodiments of the invention. Persons of ordinary skill in the art will recognize, however, that the invention can be practiced without one or more of the specific details. In other instances, well-known details are not shown or described to avoid obscuring aspects of the invention.

The present invention relates to an advanced probe card with an anti-wafer structure. Advanced probe cards and anti-wafer structures are also disclosed in U.S. Application Nos. 10/144,676 and 10/209,088, which are incorporated herein by reference in their entirety.

FIG. 1 schematically shows an anti-wafer 100 in accordance with an embodiment of the present invention. Anti-wafer 100 may include a plurality of probe dice 110, only

a few of which are labeled in FIG. 1 in the interest of clarity. Each probe die 110 is a mirror image of a die on an uncut wafer being tested. Anti-wafer 100 may serve as a probe of an advanced probe card. In other words, anti-wafer 100 provides an interface between the test equipment (also referred to as a "tester") and the wafer under test. FIG. 1 shows the probe side of anti-wafer 100, which is the side facing the wafer under test. The other side of anti-wafer 100 faces the tester. As will be more apparent below, the probe side of anti-wafer 100 may touch down on a wafer under test using a removable electrical connection, such as a vertical elastomer. This advantageously allows testing of several dies in one touch down, thereby increasing the throughput of the test process. Furthermore, because probe dice 110 are mirror images of dice under test, probe dice 110 are relatively easy to line up for testing.

FIG. 2 schematically shows a probe die 110 in accordance with an embodiment of the present invention. The probe die shown in FIG. 2 may be the one bounded by dashed circle 104 shown in FIG. 1. As shown in FIG. 2, a probe die 110 may include a plurality of pads 102. In one embodiment, each pad 102 is aligned with a corresponding pad on a die of a wafer under test. For example, if a die being tested has 100 pads, a probe die 110 may also have 100 pads that are aligned with the pads of the die. However, a probe die 110 does not necessarily have to have the same number of pads as the die. That is, in some cases, some pads on a die may not be testable. In those cases, a probe die 110 may only have pads 102 that are aligned with the testable pads.

Pads 102 provide an electrically conductive surface on the probe side of an anti-wafer 100. Pads 102 may be coupled to circuitry in the anti-wafer 100 or directly to terminals or other pads on the tester side of the anti-wafer. A pad 102 may have a hole

through which an interconnect line 103 may be formed. An interconnect line 103 may comprise an electrically conductive material for connecting a pad 102 to circuitry in the anti-wafer or to another node, such as other terminals or pads.

FIG. 3 schematically shows a cross-sectional view of an advanced probe card in accordance with an embodiment of the present invention. The advanced probe card may comprise an anti-wafer 110, a ceramic disk 305, and a printed circuit board (PCB) 304. Anti-wafer 100, ceramic disk 305, and PCB 304 may be glued or bonded together, for example. Other means of holding the aforementioned components of the advanced probe card together may also be employed without detracting from the merits of the present invention. The use of an anti-wafer, disk, and PCB advantageously allows the advanced probe card to be relatively thin and compact, thereby reducing parasitic effects, such as wire inductance, between the tester and the wafer under test.

The advanced probe card may be used in conjunction with a vertical elastomer 308 to test the dice of a wafer 350. Elastomer 308 comprises a plurality of vertically oriented electrically conductive connectors 309. Note that only some connectors 309 are labeled in FIG. 3 to avoid cluttering the figure. When elastomer 308 is compressed between anti-wafer 110 and wafer 350, connectors 309 make an electrical connection between pads 102 of anti-wafer 110 and corresponding pads 306 of wafer 350. By providing a compressible and relatively smooth connection, elastomer 308 minimizes damage to wafer 350. Elastomer 308 may be permanently attached to anti-wafer 110 using a high-temperature adhesive, for example. Elastomer 308 may also be manually placed between anti-wafer 110 and wafer 350 just prior to testing.

Ceramic disk 305 provides heat insulation between PCB 304 and anti-wafer 110. Ceramic disk 305 advantageously allows the advanced probe card to operate at relatively high temperature test environments. Holes 302 through anti-wafer 110, ceramic disk 305, and PCB 304 allow interconnect lines 103 to couple pads 102 to the side of PCB 304 facing the tester (not shown). Lines 103 may comprise wires, for example. In that case, lines 103 may be soldered on terminals, connectors, pads, or other nodes on the tester side of PCB 304. Cables (not shown) from the tester may be connected to lines 103 by way of a soldered connection or removable connector on PCB 104, for example. This allows the tester to send and receive signals to and from wafer 350. The advanced probe card may have a plurality of holes 302. For example, as shown in the cross-sectional view of FIG. 4, anti-wafer 110 may have several holes 302 for accommodating interconnect lines 103. A hole 302 through anti-wafer 110, ceramic disk 305, and PCB 304 advantageously allows for a relatively short interconnect line 103. This minimizes parasitic effects on the interconnect line.

In the example of FIG. 3, pads 102 are directly coupled to the other side of anti-wafer 110. However, pads 102 may also be coupled to circuitry within anti-wafer 110. FIG. 5 shows a portion of an advanced probe card in accordance with an embodiment of the present invention. In the example of FIG. 5, anti-wafer 110 comprises an isolation layer 110-1, a first level 110-2, and a second level 110-3. Isolation layer 110-1 may be an oxide layer (e.g., silicon on insulator layer), for example. A level of anti-wafer 110 may include electrical circuitry, such as circuit 560 in level 110-2. Circuit 560 advantageously allows off-loading of some test or signal conditioning functions to anti-wafer 110. For example, circuit 560 may be configured to include buffer and driver

circuits to condition signals coming from or being transmitted to wafer 350. As another example, circuit 560 may be similar to the BIST (built-in self-test) portion of a die under test. Note that because anti-wafer 110 may comprise silicon, conventional semiconductor fabrication techniques may be employed to incorporate circuitry in the anti-wafer.

Still referring to FIG. 5, level 110-3 may be an “adapter layer” for adopting the layout of pads 102 (which mirrors the layout of the pads of the wafer under test) to another layout that is more suitable for connecting to larger wirings, such as cables leading to the tester, for example. Note that adapting the layout of pads 102 to another layout may also be done on a single level. For example, pads 561 may be on level 110-2. In the example of FIG. 5, pads 102 are coupled to larger pads 561. This is especially advantageous in applications where pads 102 are closely spaced together and not all of them are employed during test. Interconnect lines 103 in holes 302 are not shown in FIG. 5 in the interest of clarity.

FIGS. 6-11 systematically illustrate the fabrication of an anti-wafer in accordance with an embodiment of the present invention. Referring to FIG. 6, a silicon substrate 510, a silicon on insulator (SOI) layer 508, and a chip 506 may form a silicon on insulator structure. In that case, SOI layer 508 may be an oxide layer, while chip 506 may comprise silicon in which integrated circuits and pads 102 may be fabricated. The use of a silicon on insulator structure advantageously minimizes parasitic effects, thereby allowing the anti-wafer to operate at relatively high speeds. Furthermore, the silicon on insulator structure advantageously isolates the probe side of the anti-wafer from the other components of the advanced probe cards, and isolates the pins/pads of

the anti-wafer from each other. Note that only one chip 506 is shown on the figures for clarity of illustration. It should be noted that there may be several chips 506 on SOI layer 508, with each chip 506 serving as a probe die.

In the example of FIG. 6, pad openings 507 represent etched portions of chip 506. Pad openings 507 may be formed during a pad open etch step to allow conductors to be coupled to the chip during packaging. In the present embodiment, pad openings 507 are not filled-in with a conductive material in this step. To protect pad openings 507 during subsequent processing of the anti-wafer, a silicon dioxide seal layer 504 and a silicon nitride seal layer 502 are formed over the pad openings.

In FIG. 7, substrate 510 is removed to expose SOI layer 508. In one embodiment where substrate 510 is a silicon substrate, substrate 510 may be removed using a backside polish step. The sample of FIG. 7 may be subjected to an HF dip process to clean the surface of an oxide SOI layer 508 after the polishing step. The HF dip process may remove some of SOI layer 508. For example, about 10 Angstroms to about 500 Angstroms of oxide may be removed from SOI layer 508 by the HF dip process.

In FIG. 8, which shows the sample as being turned over, additional oxides are deposited on SOI layer 508 to compensate for the ones that may have been removed in the HF dip process. Nitride seal layer 502 is then removed.

In FIG. 9, a pad mask resist 510 is formed over SOI layer 508. Pad mask resist 510 provides a pattern for etching through pad openings 507. SOI layer 508 and chip 506 are then etched through pad openings 507. This forms openings 910 from pad

mask resist 510, through SOI layer 508, and through chip 506. Only oxide seal layer 507 blocks openings 910 in FIG. 9.

In FIG. 10, oxide seal layer 504 and pad mask resist 510 are removed. Removal of oxide seal layer 504 exposes chip 506. Viewing the sample of FIG. 10 right side up, chip 506 is on SOI layer 508 with openings 910 through them. That is, openings 910 may serve as contact holes through chip 506. (Note that pad openings 507 are openings through chip 506.)

In FIG. 11, a bump process is used to form electrically conductive connections 515 through chip 506. Connections 515 may be part of interconnect lines 103 (see FIG. 3), for example. The sample of FIG. 11 may be used as anti-wafer in an advanced probe card, such as that shown in FIG. 3. While designed for a probe card in this example, the just described process could also be used in stacked-die packaging configurations or in pressure sensors, for example.

While specific embodiments of the present invention have been provided, it is to be understood that these embodiments are for illustration purposes and not limiting. Many additional embodiments will be apparent to persons of ordinary skill in the art reading this disclosure.